

An Analytical Model of Packet-Switching Finite-Buffered Multistage Interconnection Networks

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Abstract

In the past, the modeling and analyses of packet-switching, finite-buffered, multistage interconnection networks (MINs) have always considered the existence of a single buffer queue for each point in a Switching Element (SE). However, as a result of the rapid changes in the computational and information processing requirements, different configurations of machines and prioritizing of requests have become apparent. Some of these requirements necessitate the existence of different queuing techniques to handle requests based on their origination points. This paper presents the performance analysis of an analytical model of packet-switching, finite-buffered, multistage, interconnection networks. It uses very realistic assumptions and takes into account the dependencies between packets in consecutive clock cycles and between states of buffers in adjacent stages. It is developed for MINs with SEs of arbitrary sizes. It employs two buffer queues and a priority for each site to distinguish between requests that originated locally or remotely. We use throughput as the performance measure with respect to the sizes of the buffer queues and request rate of each site.

1 Introduction

The next generation of distributed computing systems will emphasize on the utilization of various MIN topologies for interconnecting a number of machines for high performance, scalable, distributed computing. Those new configurations bring with them additional properties and characteristics that are not part of the analytical parameters for conventional systems. Consequently, it becomes imperative that we develop analytical models for studying the performance analysis of various interconnection networks that may be applicable for such system configurations.

Packet switching MINs have been utilized for the interconnections between processors and main memory modules for such computing environments as large scale multiprocessor systems. Many different types of MINs have been proposed and developed ranging from blocking and non-blocking to re-arrangeable MINs. One of the earliest studies on the performance of MINs is shown in [1] which proposes a probabilistic approach to the performance analysis of a multiprocessor system using a synchronous circuit switched MIN. However, the proposal is limited to unbuffered circuit switched MINs. Several approaches have been proposed to increase the performance of unbuffered MINs such as the use of multiple links and networks [2]. Another alternative is to use buffering at each switching element (SE) such that packets that could have been lost can be saved. Several performance analyses studies have been done for buffered MINs. In [3] and [4], the analyses of single-buffered MINs with 2×2 SEs are presented. In [5] and [6], extensions of single-buffered MINs to multiple (finite) buffered MINs with SEs of arbitrary sizes are discussed. Due to the low accuracies in those analyses when input load is high or their restrictive applicabilities, [7] presents a new model for the performance evaluation of finite-buffered multistage interconnection

networks. A more realistic model is presented which takes into account the dependencies between packets in consecutive clock cycles and between states of buffers in adjacent stages.

Other modeling assumptions have been utilized for the analysis of MINs. In [2, 8], the performance of MINs with buffers of infinite size is presented while [9, 10] also study infinite-buffered MINs with different modeling assumptions.

In this paper, an analytical model of evaluating finite-buffered MINs with SEs of arbitrary sizes is presented. Due to the morphology of the configuration of the proposed network topology, two types of buffer queues are utilized for requests that originate locally or remotely. Most of the modeling assumptions follow those presented in [7]. We use throughput as the performance measure with respect to the buffer queue sizes and request rate of each site.

2 The Interconnection Network Model

The network model is a packet-switching network based on a class of MINs called *delta network* [1]. It employs the concept of a *node* which is a collecting of sites. A site is similar to a single input source in a circuit switching network. A node is similar to the classical concept of a Processing Element (PE). Within each node, there is a number of channels (output sources as in circuit switches). A request going through any of the sites in a node uses one of the channels to get to another site in another node, in the next stage. A stage is a collection of nodes that are processed simultaneously to determine the next destination of a request. A request enters the network at any stage with probability m , the request rate. A request at its generation stage is called an *internal request* and it is stored in an *internal buffer queue*. A request arriving from a different stage is called an *external request* and it is stored in the *external buffer queue*. There is a ratio between the maximum number of internal or external requests that a site can accumulate. If a site generated a request and the number of internal requests in the internal buffer queue for that site has reached the maximum as determined from the ratio, then that site's current request is discarded or ignored.

2.1 Determining Requests to Satisfy

During each stage cycle, decisions must be made between the requests in the buffer queues to select the requests that should proceed to the next stage. In order to determine the queue from which a request is selected for a given site, the model requires that a priority be given between the internal and external requests. If the external requests were given a higher priority, then a request is taken from the site's external buffer queue, if it were not empty. If the external buffer queue was empty, and the internal buffer queue has some requests, then a request is taken from the internal buffer queue. Conversely, if the internal requests were given a higher priority, then the same rule applies with preference given to the site's internal buffer queue. The maximum number of requests allowable in an internal buffer queue is expressed as a fraction of the maximum size of the external buffer.

Once all the requests have been selected, a conflict resolution is conducted among all the requests leaving a particular node. A conflict exists between two or more requests if they are trying to use the same channel from their node. One of these competing requests is selected at random while the others are blocked.

2.2 Inter Stage Migrations of Requests

After selecting all the non-conflicting requests, a request can only move to its next stage destination if certain conditions are met. If the current stage cycle was the last stage of the network, then the number of non-conflicting requests contributes to the throughput of the network, and those requests are subsequently removed from their respective buffer queues. However, if it were not the last stage, then each request tries to move forward. A request

can only move forward if there is space for it in the next stage's destination site's buffer queue. If the destination site's external buffer queue is not full, then the request is added to the site's external request buffer queue and subsequently removed from the originating buffer queue. A non-conflicting request that could not move forward is stored in a pending buffer queue in the site. This indicates that the request wants to move forward if a request in the next stage destination site's external buffer queue was able to move forward.

At the completion of a cycle, i.e., getting to the last stage, a scan is done backwards to determine if any of the pending requests could move forward, eventually. If any was able to move forward, it is subsequently removed from its current stage site's buffer queue. An $a^n \times a^n$ MIN consists of n stages of SEs where each SE is an $a \times a$ crossbar. Figure 1 shows two network nodes that belong to different stages with samples of requests for the internal and external buffer queues. Each node is a 3×3 node. In the first node, N_1 , we assume that S_1 made two requests, $R1, R2$, and S_3 made two requests, $R3, R4$. In the second node, N_2 , we assume that S_1 made $R5$ request and S_2 made $R6$ request. If the current stage cycle is t , then the requests by N_1 were made at $(t-1)$ th stage cycle and N_2 requests were made at the current stage cycle. Therefore, at the $(t-1)$ th stage cycle, following the requests by N_1 , its internal buffer queue contains the requests $\{R1, \dots, R4\}$. If $R4$ won the contention during the $(t-1)$ th stage cycle and its next node destination is N_2 , then it is stored in N_2 's external buffer queue. The figure also shows the buffering of the local requests generated at t th stage cycle by N_2 sites.

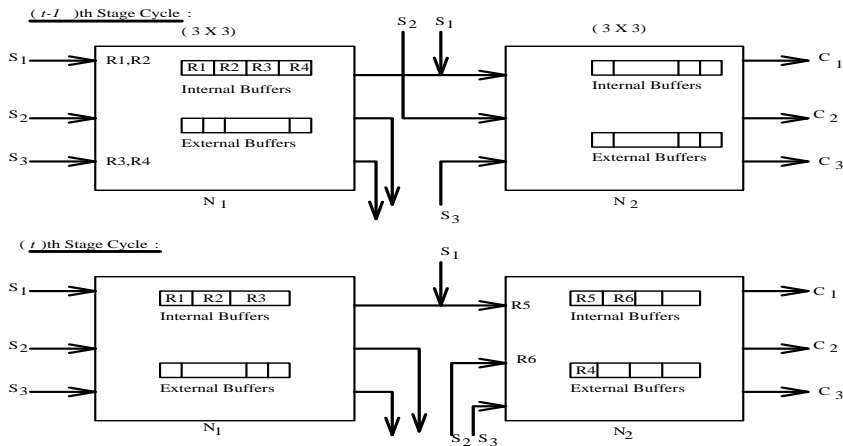


Figure 1: Network nodes showing buffer queues and requests migrations.

3 Network Analysis

As a prelude to the definition of the functional probabilities of the network, we enumerate some other assumed characteristics of the network. These include:

- Each node comprises the same number of local sites and channels,
- Packets are generated by each site at each node with equal probability,
- Packets are uniformly distributed to the destination points,
- Conflicts are randomly resolved,
- Packets are selected from the buffer queues on First-Come-First-Served basis,
- There is a finite number of packets that are allowed in the network,

- Each local site can generate a request at each stage cycle,
- There is a priority that determines which packet to select for transmission at each stage cycle, for both locally generated or remotely generated requests.

At the beginning of each stage cycle, each local site generates a request. If the site has not used up its ability to store locally generated requests, then the request is stored in the internal buffer queue.

A packet goes through three phases on its movement from one stage to the other:

1. In the first phase, packets are selected from either the internal or external buffer queue according to the priority specified.
2. In the second phase, conflicts are resolved, and the movability of a packet is determined. A selected packet can move forward if its destination site's buffer queue is not full or a packet in the destination site can move forward.
3. Finally, the packet moves forward one stage.

In order to analyze the throughput of our network, various variables are necessary. The following are the definitions of those variables:

- n = Number of switching stages in the network.
- a = Number of sites per node.
- b = Number of channels per node.
- e = Maximum number of external requests per site.
- r = Fractional value for maximum size of an internal buffer queue with respect to the size of the external buffer ($0 < r < 1$).
- p = Priority. $p = 1$ implies that external requests have higher priority; otherwise, internal buffer queues have priority.

3.1 Definitions of Probabilities

The definitions of the necessary probability values for the network analysis are presented below. We first define the probabilities for general network routing followed by those for internal and external buffer queues. Therefore,

$q(k, t)$ = probability that a packet is ready to come to a buffer queue of a site at stage k during the t th stage cycle.

$r(k, t)$ = probability that a packet in a buffer queue at stage k is able to move forward to the desired output port during the t th stage cycle by winning the contention among competing packets, given that the nodal buffer queues are not empty.

$n_0(k, t)$ = probability that the nodal buffer queues of a site at stage k are empty during the t th stage cycle.

3.2 Definitions for Internal Buffers

We now define the probability values associated with the internal buffer queues:

$p_j^{int}(k, t)$ = probability that there are j packets in an internal buffer queue of a site at stage k during t th stage cycle where $0 \leq j \leq er$.

$p_0^{int}(k, t)$ = probability that the internal buffer queue of a site at stage k is empty during the t th stage cycle.

$p_1^{int}(k, t)$ = probability that the internal buffer queue of a site contains only one packet during the t th stage cycle.

$p_{full}^{int}(k, t)$ = probability that the internal buffer queue of a site in stage k is full during the t th stage cycle, i.e., it contains er buffer requests.

$f^{int}(k, t)$ = probability that a packet in an internal buffer queue of a site at stage k is able to move forward to the next stage during the t th stage cycle given that the internal buffer queue is not empty.

$p^{int}(k, t)$ = Probability that a site in stage k makes a request during the t th stage cycle.

3.3 Definitions for External Buffers

The following are the probabilities associated with external buffers:

$p_0^{ext}(k, t)$ = probability that the external buffer queue of a site at stage k is empty during the t th stage cycle.

$p_j^{ext}(k, t)$ = probability that there are j packets in an external buffer of a site at stage k during the t th stage cycle where $0 \leq j \leq e$. (p_e^{ext} is similarly defined to indicate when the buffer queue is full)

$p_1^{ext}(k, t)$ = probability that the external buffer of a site contains only one packet during the t th stage cycle.

$f^{ext}(k, t)$ = probability that a packet in an external buffer of a site at stage k is able to move forward to the next stage during the t th stage cycle given that the external buffer is not empty.

3.4 Derivations of Probability Values

From the definitions above, we now derive the actual values of the applicable and necessary variables.

(1) The chances that a packet is ready to come to a buffer of a site at stage k during the t th stage cycle depends on the probability that an output (channel) at stage $k - 1$ has a request.

That is,

$$q(k, t) = [1 - (1 - [\bar{n}_0(k - 1, t)/b]^a)], \quad 2 \leq k \leq n + 1. \quad (1)$$

3.4.1 Probabilities for Empty Buffers

(2) A nodal buffer of a site is empty if

- no packet was ready to come to the site and
 - both the internal and external buffers were empty or
 - a packet from the non-empty buffer queue was able to move forward.

That is,

$$\begin{aligned} n_0(k, t) = & \bar{q}(k, t) [p_0^{int}(k, t)p_0^{ext}(k, t) + p_1^{ext}(k, t)f^{ext}(k, t)p^{int}(k, t) \\ & + p_0^{ext}(k, t)p_1^{int}(k, t)f^{int}(k, t)] + \bar{p}[p_1^{int}(k, t)f^{int}(k, t)p^{ext}(k, t) + \\ & p_0^{int}(k, t)p_1^{ext}(k, t)f^{ext}(k, t)]], \quad 1 \leq k \leq n. \end{aligned} \quad (2)$$

(3) The probability that an internal buffer queue is empty depends on whether

- a request was generated by the site during the current stage cycle and
 - if the internal buffer queue was already empty or
 - if the internal buffer queue had one packet that was able to move forward.

Therefore,

$$p_0^{int}(k, t + 1) = \bar{p}^{int}(k, t)[p_0^{int}(k, t) + p_1^{int}(k, t)f^{int}(k, t)], \quad 1 \leq k \leq n. \quad (3)$$

(4) The probability that an external buffer is empty depends on whether

- a request was ready to come to the site during the current stage cycle and
 - if the external buffer was already empty or
 - if the external buffer had one packet that was able to move forward.

Therefore,

$$p_0^{ext}(k, t + 1) = \bar{q}(k, t)[p_0^{ext}(k, t) + p_1^{ext}(k, t)f^{ext}(k, t)], \quad 1 \leq k \leq n. \quad (4)$$

3.4.2 Probabilities for Inter Stage Migratability

(5) The probability that a packet in a nodal buffer at stage k is able to pass the node to the desired destination in the next stage having won the contention depends on whether a packet is ready to come to the external buffer of the destination site at stage $(k + 1)$ during the t th stage cycle given that the source buffers were not empty. That is,

$$r(k, t) = \frac{q(k + 1, t)}{\bar{n}_0(k, t)}, \quad 1 \leq k \leq n - 1. \quad (5)$$

(6) The probability that a packet in an external/internal buffer is able to move to the next stage depends on

- the packet winning the contention and
 - there being a space for it in the destination site's buffer or
 - one of the packets in the destination site being able to move forward.

In other words,

$$f^{ext}(k, t) = r(k, t)[\bar{p}_e^{ext}(k + 1, t) + p_{ext}^{ext}(k + 1, t)f^{ext}(k + 1, t)], \quad 1 \leq k \leq n - 1. \quad (6)$$

$$f^{int}(k, t) = r(k, t)[\bar{p}_e^{ext}(k + 1, t) + p_e^{ext}(k + 1, t)f^{ext}(k + 1, t)], \quad 1 \leq k \leq n - 1. \quad (7)$$

$$f(n, t) = [1 - ([1 - \bar{n}_0(n, t)/a]^a / \bar{n}_0(n, t))]. \quad (8)$$

3.4.3 Probabilities for Buffer Accumulations

(7) The probability that there are j packets in the internal buffer of a site at stage k during the $(t + 1)$ th stage cycle depends on

- whether the site generated a new request during this stage cycle,
- the number of packets already in the buffer and
- whether any one of the packets in the buffer queues was able to move forward.

That is,

$$p_j^{int}(k, t + 1) = p^{int}(k, t)[p_{j-1}^{int}(k, t)\bar{f}^{int}(k, t) + p_j^{int}(k, t)f^{int}(k, t)] + \bar{p}^{int}(k, t)[p_j^{int}(k, t)\bar{f}^{int}(k, t) + p_{j+1}^{int}(k, t)f^{int}(k, t)], \quad 2 \leq j \leq m - 1, \quad 1 \leq k \leq n. \quad (9)$$

(8) The probability that there are j packets in the external buffer of a site at stage k during the $(t + 1)$ th stage cycle depends on whether

- a packet is ready to come to the site during the t th stage cycle and
 - if a packet was able to move forward from the site during the current cycle.

That is,

$$\begin{aligned}
 p_j^{ext}(k, t+1) &= q(k, t)[p_{j-1}^{ext}(k, t)\bar{f}(k, t) + p_j^{ext}(k, t)f(k, t)] + \\
 &\quad \bar{q}(k, t)[p_j^{ext}(k, t)\bar{f}(k, t) + p_{j+1}^{ext}(k, t)f(k, t)], \\
 2 \leq j \leq m-1, \quad 1 \leq k \leq n.
 \end{aligned} \tag{10}$$

3.4.4 Probabilities for Single Buffer Accumulations

(9) The probability that there is only one packet in an internal buffer of a site at stage k during the $(t+1)$ th stage cycle depends on whether

- the site made a request during this stage cycle, and
 - the internal buffer is empty and the new packet was not able to move forward or,
 - there was one packet in the internal buffer and it was able to move forward,
- the site did not make a request and,
 - there was only one packet in the internal buffer and it was not able to move forward, or
 - there were two packets in the buffer and one was able to move forward.

That is,

$$\begin{aligned}
 p_1^{int}(k, t+1) &= p^{int}(k, t)[p_0^{int}(k, t)\bar{f}^{int}(k, t) + p_1^{int}(k, t)f^{int}(k, t)] + \\
 &\quad \bar{p}^{int}(k, t)[p_1^{int}(k, t)\bar{f}^{int}(k, t) + p_2^{int}(k, t)f^{int}(k, t)], \\
 1 \leq k \leq n.
 \end{aligned} \tag{11}$$

(10) The probability that there is only one packet in an external buffer of a site at stage k during the $(t+1)$ th stage cycle depends on whether

- a packet is ready to come to the external buffer of the site during the current stage cycle, and
 - the external buffer is empty and the new packet was not able to move forward,
 - there was one packet in the external buffer and it was able to move forward,
- a packet is not ready to come to the site and,
 - there was only one packet in the external buffer and it was not able to move forward, or
 - there were two packets in the external buffer and one was able to move forward.

Therefore,

$$\begin{aligned}
 p_1^{ext}(k, t+1) &= q(k, t)[p_0^{ext}(k, t)\bar{f}^{ext}(k, t) + p_1^{ext}(k, t)f^{ext}(k, t)] + \\
 &\quad \bar{q}(k, t)[p_1^{ext}(k, t)\bar{f}^{ext}(k, t) + p_2^{ext}(k, t)f^{ext}(k, t)], \quad 1 \leq k \leq n.
 \end{aligned} \tag{12}$$

3.4.5 Probabilities for Full Buffers and Throughput

(11) The probability that an internal buffer of a site at stage k is full during the $(t + 1)$ th stage is contingent upon

- the site making a request during the current stage cycle and,
 - the buffer was one packet less than full and none of the packets moved forward, or
 - the buffer was full and one of the packets moved forward,
- the site making no request during the current stage cycle and,
 - the buffer was full and no packet moved forward.

That is,

$$p_{full}^{int}(k, t + 1) = p^{int}(k, t)[p_{er-1}^{int}(k, t)\bar{f}^{int}(k, t) + p_{full}^{int}(k, t)f^{int}(k, t)] + \bar{p}^{int}[p_{full}^{int}(k, t)\bar{f}^{int}(k, t)], \quad 1 \leq k \leq n. \quad (13)$$

(12) The probability that an external buffer of a site at stage k is full during the $(t + 1)$ th stage is contingent upon

- a packet being ready to come to the buffer of the site during the current stage cycle and,
 - the buffer was one packet less than full and none of the packets moved forward, or
 - the buffer was full and one of the packets moved forward
- no packet coming to the site during the current stage cycle and,
 - the buffer was full and no packet moved forward.

Therefore,

$$p_e^{ext}(k, t) = q(k, t)(k, t)[p_{e-1}^{ext}(k, t)\bar{f}^{ext}(k, t) + p_e^{ext}(k, t)f^{ext}(k, t)] + \bar{q}(k, t)[p_e^{ext}(k, t)\bar{f}^{ext}(k, t)], \quad 1 \leq k \leq n. \quad (14)$$

The *throughput* (**TP**) is the average number of packets delivered by a MIN in a stage cycle. It is derived from $q(n + 1)$ and b^n as follows:

$$TP = q(n + 1)b^n. \quad (15)$$

4 Simulation Model

The primary goals of the simulation are to analyze the throughputs of the network model in comparison with related models and to understand the impacts of its unique characteristics to the network throughputs. Specifically, we will like to analyze the effects of the buffer sizes, request rate, priority, and request ratio.

4.1 Simulation Parameters

The simulation model used is based on the delta network. Each simulation consists of a network of a given dimension, number of stages, request rate, and maximum stage cycles. The dimension represents the configuration of every node in the network. The number of stages represents the maximum actual stage transitions for each request before getting to its destination. The request rate is the probability that a request is valid and acceptable. During each stage cycle, a site generates a random number between 0 and 1. That value represents the indication that the site wants to make a request. If the value is within the request rate, relative to zero, then the request is acceptable. Subsequently, a destination address is generated for the request. A destination address is a random number which is normalized to a possible value within the total number of channels of the nodes in the last stage of the network. The requests are then routed through the network according to the delta network routing protocols. The number of requests that arrive at the last stage are accumulated for determining the average bandwidth of the network. A number of simulations are carried out with different parameters, however, due to the behavioral similarities between the simulations, we present a generalized analysis.

4.2 Analysis of Simulation Results

With respect to the peculiar characteristics of a network, we analyze its behavior as it relates to its bandwidth.

4.2.1 High Throughput

In order to understand the motivation for the model of the network, we present the analysis of its throughput vis-à-vis related networks. One of the conspicuous attributes of the simulation results is the high throughput of the network as evidenced in Figure 2. This is as expected since each site at each node tries to generate a request at each stage cycle. This increases the chances that a request is ready to come to another site in the next stage. Originally, from [2], the probability that a request is ready to come to a buffer is defined as

$$q(k, t) = 1 - [1 - \bar{p}_0(k - 1, t)/a]^a$$

where \bar{p}_0 is the probability that the buffer is empty.

From the definition of $q(k, t)$ above, it is evident that the probability that a nodal buffer is empty is less in this model than the model presented in [2]. That is,

$$[1 - n_0(k, t)] \geq [1 - p_0(k, t)]$$

This accounts for the higher *TP* for this model. Figure 2 shows a comparison of the throughputs between two network models. The referenced model refers to the network presented in [7] whose analysis method is similar to the one presented here.

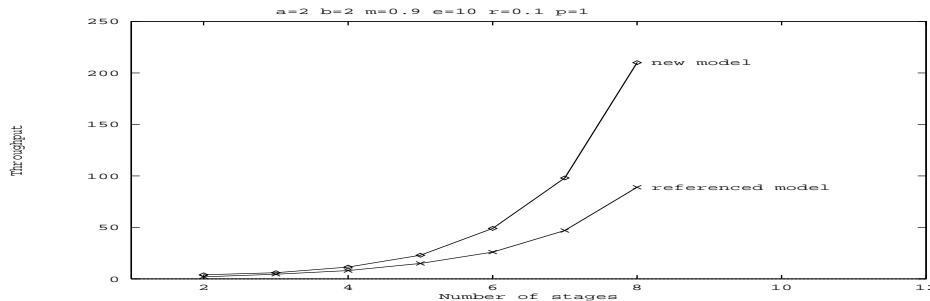


Figure 2: A comparison of throughput and number of stages.

4.2.2 Ratio vs Throughput

As the internal and external buffer sizes increase, the throughput increases to a certain level and then becomes fairly stable as Figure 3 indicates. For example, the throughput increased when the ratio increased from 0.1 to 0.2 because with the increase, the network was able to use another packet when only one packet was able to come to the node. A ratio of 0.1 in the simulation is equivalent to the model presented in [2] and so had lower TP . However, as the ratio increased, the TP increased until the effect of the existence of requests in the internal buffers became inconsequential. If the external request had higher priority and an external request is blocked for a particular channel, it does not matter whether there are requests in the external buffer; no request can proceed through that channel. Therefore, as the network got more congested, the TP either decrease slightly or leveled.

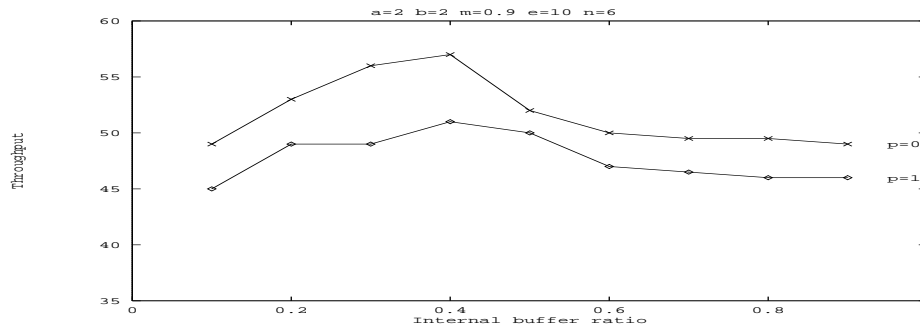


Figure 3: A comparison of throughput and internal buffer ratio.

4.2.3 Ratio vs Request rate

The fact that the TP increased as the ratio remained constant and the request rate increased is not surprising in view of the descriptions given above. As the request rate increased, the probability that a site will generate a request increased, thereby increasing the total number of requests in the system and the TP consequently. However, as the network became congested with requests, the throughput decreased slightly due to the increase in the probability of blocked requests and then became static because additional requests do not increase the chances of more requests being able to move forward. These behaviors are captured in Figure 4.

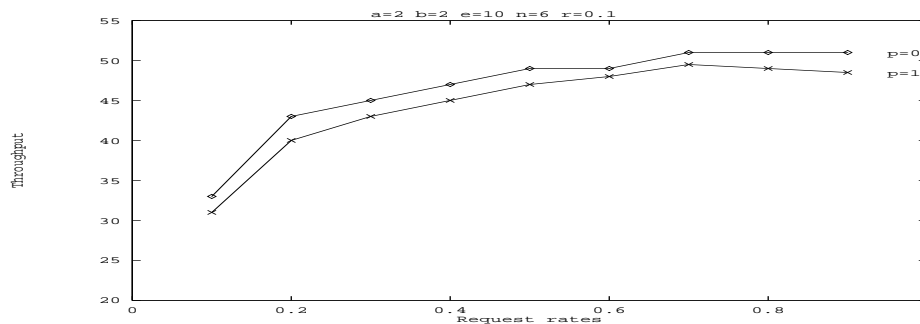


Figure 4: A comparison of throughput and request rate.

5 Conclusions

In this paper, we present an analysis of an analytical model of a packet-switching finite-buffered multistage interconnection network. We describe a network model based on the

delta network where each SE consists of sites and channels (input and output sources). Each SE (node) is associated with internal and external buffers. The internal buffers store requests that are generated locally by a site while external buffers store those requests that are generated in the preceding stages by other sites. The maximum size of the internal buffers is specified as a ratio of the internal buffer size. We present the routing process for requests in the network and the probabilistic analysis of request migrations to their destinations. A limited, but sufficient, schematic of the transition states is also presented. A simulation model is built on the network model and the results discussed with respect to the throughputs in general, buffer sizes vis-à-vis the throughputs, and buffer sizes vis-à-vis the request rates. The model and results indicate the effects of the existence of multiple buffer queues on a system's throughput and an efficient way of handling such network topologies in the presence of similar requirements.

References

- [1] **J.H. Patel**, Performance of Processor-Memory Interconnections for Multiprocessors, *IEEE Trans. Computers*, vol. C-30, No. 10, pp. 771-780, Oct. 1981.
- [2] **C.P. Kruskal and M. Snir**, The performance of multistage interconnection networks for multiprocessors, *IEEE Trans. Computer*, vol. C-32, no. 12, pp. 1091-1098, Dec. 1983.
- [3] **D.M. Dias, J.R. Jump**, Analysis and simulation of buffered delta networks, *IEEE Trans. Computers*, vol. C-30, no. 4, pp. 273-282, Apr. 1981.
- [4] **Y. Jenq**, Performance Analysis of a Packet Switch Based on Single-Buffered Banyan Network, *IEEE J. on Selected Areas in Comm.*, vol. sac-1, no. 6, pp. 1014-1021, Dec. 1983.
- [5] **M. N. Huber, E. P. Rathgeb, T. H. Theimer**, Banyan Networks in an ATM-Environment, *Proc. ICC'88*, Tel Aviv, Israel, pp. 167-174, 1988.
- [6] **H. Yoon, K.Y. Lee, M.T. Liu**, Performance Analysis of Multibuffered Packet-Switching Networks in Multiprocessor Systems, *IEEE Trans. Computers*, vol. 39, No. 3, pp. 319-327, Mar. 1990.
- [7] **S. Hsien, C. Y. R. Chen, K. C. Nwosu, D. Meliksetian**, Performance Analysis of Finite-Buffered Multistage Interconnection Networks, *Proc. International Conference on Communications (ICC'93)*, pp. 53-57, Geneva, Switzerland, May 23-26, 1993.
- [8] **C. P. Kruskal, M. Snir, A. Weiss**, The Distribution of Waiting Times in Multistage Interconnection Networks, *IEEE Trans. Comput.*, vol. c-37, pp. 1337-1352, Nov. 1988.
- [9] **H. Jiang, L. N. Bhuyan, J. K. Muppala**, MVAMIN: Mean Value Analysis Algorithm for Multistage Interconnection Networks, *Journal of Parallel and Distributed Computing*, pp. 189-201, 1991.
- [10] **D. L. Willick, D. L. Eager**, An Analytical Model of Multistage Interconnection Networks, *Proc. 1990 ACM SIGMetrics Conf.*, pp. 192-202, 1990.